Listing of the Claims:

The following is a complete listing of all the claims in the application, with an indication of the status of each:

1. (Currently amended) A multichip circuit module having a main circuit board ~~(9)~~, at least one carrier substrate ~~(1) which is~~ mounted on the main circuit board ~~(9)~~ and which is in electrical contact with the main circuit board ~~(9)~~, and at least one semiconductor chip ~~(5)~~ on the carrier substrate ~~(1)~~ which is in electrical contact with the carrier substrate ~~(1)~~, wherein

the carrier substrate ~~(1) having~~ has at least one cavity ~~(4)~~ on a mounting surface to accommodate said at least one semiconductor chip ~~(5)~~,

connecting contacts ~~(6)~~ for associated bumps ~~(7)~~ of said at least one ~~the~~ semiconductor chip ~~(5) being~~ are provided in said at least one ~~the~~ cavity ~~(4)~~,

the at least one semiconductor chip ~~(5)~~ being mounted on the connecting contacts ~~(6)~~ by using the associated bumps in a ~~the~~ flip-chip technique, and

the mounting surface ~~(3)~~ of the carrier substrate ~~(1)~~ being applied to a contact surface ~~(10)~~ of the main circuit board ~~(9)~~ and the mounting surface ~~(3)~~ of the carrier substrate ~~(1), characteriazed in that~~ wherein the carrier substrate ~~(1)~~ has many layers with conductor tracks ~~(2)~~ extending transversely through a plurality of layers, and a ~~the~~ filling material ~~(11)~~ makes contact with a ~~the~~ rear of said at least one semiconductor chip in said at least one cavity ~~the semiconductor chips (5) in the cavities (4)~~ without enclosing the connecting contacts ~~(6)~~ and bumps ~~(7)~~.

2. (Currently amended) The multichip circuit module as claimed in claim 1, wherein ~~characterized in that~~ the filling material ~~(11)~~ is an anisotropically conductive material~~, for example an anisotropically conductive paste or an anisotropically conductive film~~.

3. (Currently amended) The multichip circuit module as claimed in claim 1 ~~or 2, characterized in that~~ wherein the filling material ~~(11)~~ does not fill the interspaces of the at least one cavity ~~cavities~~ completely.

4. (Currently amended) The multichip circuit module as claimed in claim 1 wherein the ~~one of the preceding claims, characterized in that~~ conductor tracks ~~(2)~~ of the carrier substrate ~~(1)~~ are led to the mounting surface ~~(3)~~ and are connected electrically and mechanically to conductor tracks ~~(12)~~ of the main circuit board ~~(9)~~ for the simultaneous carrying of signals, dissipation of heat, encapsulation and shielding.

5. (Currently amended) The multichip circuit module as claimed in claim 1 further comprising ~~one of the preceding claims, characterized by~~ a planar antenna arrangement ~~(8)~~ on an ~~the~~ underside of the carrier substrate ~~(1)~~, which is opposite the mounting surface ~~(3)~~.

6. (Currently amended) The multichip circuit module as claimed in claim 1 wherein ~~one of the preceding claims, characterized in that~~ the carrier substrate ~~(1)~~ is a multilayer ceramic~~, in particular a low-temperature co-fired ceramic (LTCC)~~.

7. (Currently amended) A method for production of multichip circuit modules ~~as claimed in one of the preceding claims~~ having a main circuit board, at least one carrier substrate mounted on the main circuit board and which is in electrical contact with the main circuit board, and at least one semiconductor chip on the carrier substrate which is in electrical contact with the carrier substrate, wherein

the carrier substrate has at least one cavity on a mounting surface to accommodate said at least one semiconductor chip,

connecting contacts for associated bumps of said at least one semiconductor chip are provided in said at least one cavity,

the at least one semiconductor chip being mounted on the connecting contacts by using the associated bumps in a flip-chip technique, and

the mounting surface of the carrier substrate being applied to a contact surface of the main circuit board and the mounting surface of the carrier substrate wherein the carrier substrate has many layers with conductor tracks extending transversely through a plurality of layers, and a filling material makes contact with a rear of said at least one semiconductor chip in said at least one cavity without

enclosing the connecting contacts and bumps, having the following steps:

a) letting the at least one semiconductor chip ~~(5)~~ into cavities ~~(4)~~ provided for ~~the~~ semiconductor chips ~~(3)~~ on a mounting surface ~~(3)~~ of the carrier substrate ~~(1)~~;

b) mounting the at least one semiconductor chip ~~(5) in the flip-chip technique~~ by making contact with the bumps ~~(7)~~ of the at least one semiconductor chip to ~~chips (5) resting on~~ connecting contacts ~~(6)~~ in the cavities ~~(4)~~ using a flip-chip technique;

c) applying a layer of filling material ~~(11)~~ to the contact surface ~~(10)~~ of the main circuit board ~~(9)~~; and

d) applying the carrier substrate ~~(1)~~ having the mounting surface ~~(3)~~ to the contact surface ~~(10)~~ of the main circuit board ~~(9)~~.

8. (Currently amended) The method as claimed in claim 7 wherein said applying a layer of filling material step is performed ~~, characterized~~ by application of an anisotropically conductive filling material ~~(11), in particular a paster or a film,~~ to the contact surface ~~as the filling material (11)~~.

9. (Currently amended) The method as claimed in claim 7 ~~or 8, characterized by~~ wherein said applying a layer of filling material step includes application of the filling material ~~layer (11)~~ in a layer thickness which is matched in such a way that interspaces of the cavities ~~(4)~~ are not filled completely with the filling material ~~(11)~~.

10. (Currently amended) The method as claimed in claim 7 further comprising the step of electrically connecting the ~~one of claims 7 to 9, characterized by electrical connection of~~ conductor tracks ~~(2)~~, which extend transversely through a plurality of layers of the carrier substrate ~~(1)~~ and are led to the mounting surface ~~(3)~~ to conductor tracks ~~(12)~~ of the main circuit board ~~(9)~~.

11. (Currently amended) The method as claimed in claim 7 wherein the steps are performed ~~one of claims 7 to 10, characterized by production~~ in a gas atmosphere

in order to enclose gas in the cavities ~~(4)~~.

12. (New) The multichip circuit module of claim 2 wherein said anisotropically conductive material is selected from the group consisting of an anisotropically conductive paste and an anisotropically conductive film.

13. (New) The multichip circuit module as claimed in claim 2 wherein the filling material does not fill the interspaces of the at least one cavity completely.

14. (New) The multichip circuit module as claimed in claim 6 wherein said multilayer ceramic is a low-temperature co-fired ceramic (LTCC).

15. (New) The method as claimed in claim 7 wherein said anisotropically conductive filling material is a paste or a film.

16. (New) The method as claimed in claim 8 wherein said applying a layer of filling material step includes application of the filling material in a layer thickness which is matched in such a way that interspaces of the cavities are not filled completely with the filling material.

17. (New) The method as claimed in claim 8 wherein the steps are performed in a gas atmosphere in order to enclose gas in the cavities.

18. (New) The method as claimed in claim 9 wherein the steps are performed in a gas atmosphere in order to enclose gas in the cavities.

19. (New) The method as claimed in claim 10 wherein the steps are performed in a gas atmosphere in order to enclose gas in the cavities.